## Ghoshan Jagnathamani

Lab 1

ECEN 449 - 503

Introduction

In this Lab we set up Vivado and got familiarized with the ZYNQ 7000 FPGA board. Programming in Verilog to complete the tasks in 3 sections od the lab.

Procedure/Results

Lab1 a:

We set up the development project on Vivado to do a simple operation on the board’s LED light. The implementation was that the corresponding LED had to switch on when the button was pressed. We also added a constraints file to show how each input/output matches with the corresponding component in the board.

Lab1 b:

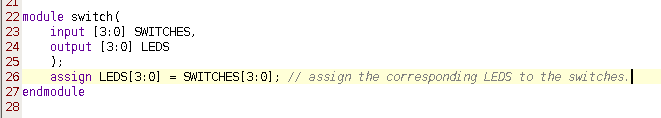
In this part we had to implement a counter. The complicated part involved creating another module to divide the clock to 1Hz so that it will count every second. Also the count had to go up or down according to the input. The output was shown on the LEDs as a 4-bit counter.

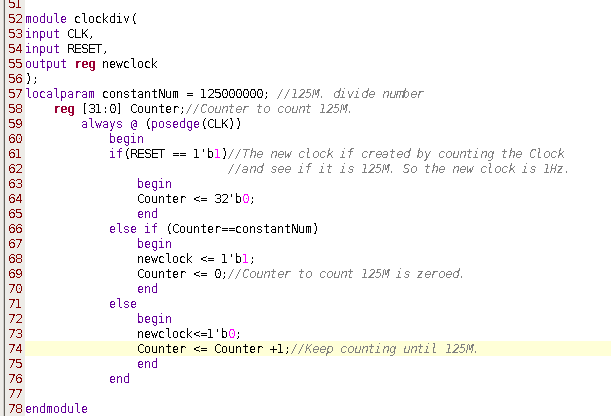
Lab1 c:

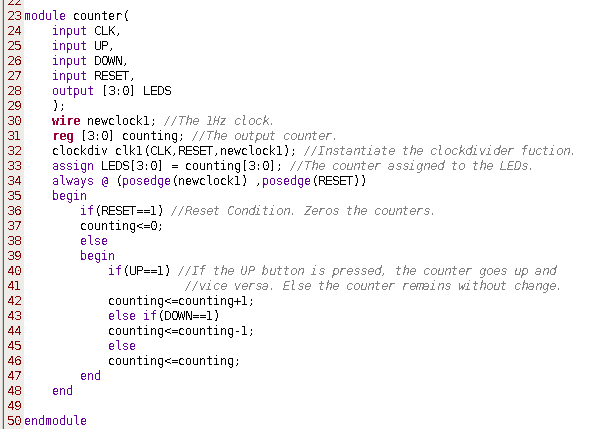
This part was to replicate the jackpot game. Again a clock divider was needed similar to the one in part b to make the light changes visible. The lights had to shift in a one hot fashion and a case was employed to do this. If the corresponding button was pressed for the light, the winning condition was provoked.

Verilog

1 a: switch.v



1 b: counter.v



Conclusion

The new things learned in this lab are

1. Vivado, development environment setting up
2. FPGA board button, light, clock
3. Verilog conditional statements.
4. Bitstream synthesis and program to board
5. Synthesizable code

Question

(a) How are the user push-buttons wired on the ZYBO board (i.e. what pins on the FPGA do each of them correspond to and are the signals pulled up or down)? You will have to consult the Master XDC file for this information.

(b) What is the purpose of an edge detection circuit and how should it have been used in this lab?